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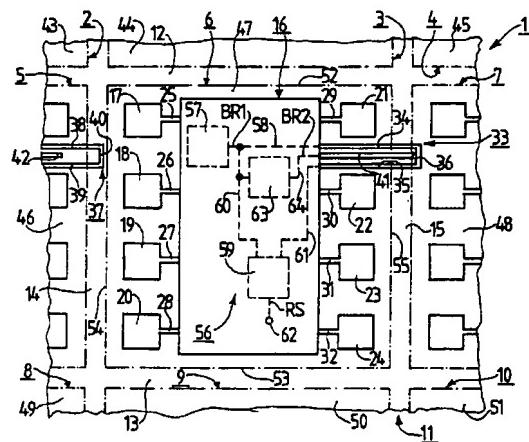
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD OF FABRICATING INTEGRATED CIRCUITS, PROVIDING IMPROVED SO-CALLED "SAW BOW" CONDUCTIVE TRACKS



(57) Abstract: An integrated circuit (6) has a semiconductor die (47) and an integrated circuit configuration (16) realized on the semiconductor die (47) and situated within bounding faces (52, 53, 54, 55) of the semiconductor die (47), in which two conductor track sections (34, 35) have been provided, which issue from the integrated circuit configuration (16) and which each extend up to a bounding face (55) and which are required for the application of a useful signal (BRI) utilized for test purposes during the fabrication of the integrated circuit (6), and in which an additional conductor track section (41) has been provided, which is disposed adjacent the two conductor track sections (34, 35) and which issues from the integrated circuit configuration (16) and extends toward a bounding surface (55) and preferably up to this bounding face (55) and which serves for the application of a spurious signal (BR2) which interferes with testing.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER IPC 7 H01L23/58
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT
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Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DE 42 00 586 A (PHILIPS PATENTVERWALTUNG) 15 July 1993 (1993-07-15) cited in the application abstract figures 1,2 claims 1-6 ---	1-6
A	EP 0 438 127 A (TOSHIBA MICRO ELECTRONICS ; TOKYO SHIBAURA ELECTRIC CO (JP)) 24 July 1991 (1991-07-24) abstract; figures 2,3 column 2, line 8 - line 27 claim 1 --- -/-	1-6

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Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 045 (E-0880), 26 January 1990 (1990-01-26) & JP 01 276735 A (FUJI ELECTRIC CO LTD), 7 November 1989 (1989-11-07) abstract; figure 1 ---	1-6
A	US 5 059 899 A (DUESMAN KEVIN ET AL) 22 October 1991 (1991-10-22) abstract; figures 1-3 column 2, line 8 - line 21 column 3, line 17 - line 40 claim 1 -----	1-6

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte nal Application No

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